

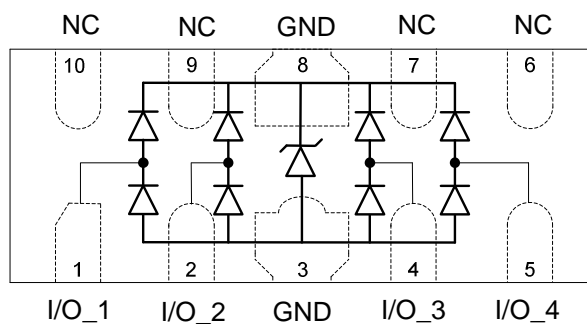
## Description

The DL0524P5-L is an ultra low capacitance TVS array, utilizing leading monolithic silicon technology to provide fast response time and low ESD clamping voltage, making this device an ideal solution for protecting voltage sensitive high-speed data lines. The DL0524P5-L has an ultra-low capacitance with a typical value at 0.2pF, and complies with the IEC 61000-4-2 (ESD) standard with  $\pm 15\text{kV}$  air and  $\pm 8\text{kV}$  contact discharge. It is assembled into a 10-pin 2.5 x 1.0x0.5mm lead-free DFN package. The flow through style package allows for easy PCB layout and matched trace lengths necessary to maintain consistent impedance between high speed differential lines such as USB 3.0 and HDMI. The small size, ultra-low capacitance and high ESD surge protection make DL0524P5-L an ideal choice to protect HDMI, MDDI, USB 3.0 and other high speed ports.

## Mechanical Characteristics

- ◆ Package: DFN2510-10 (2.5 x 1.0 x 0.5mm)
- ◆ Lead Finish: Matte Tin
- ◆ UL Flammability Classification Rating 94V-0
- ◆ Case Material: "Green" Molding Compound
- ◆ Moisture Sensitivity: Level 3 per J-STD-020
- ◆ Terminal Connections: See Diagram Below
- ◆ Marking Information: See Below

## Dimensions and Pin Configuration



Circuit and Pin Schematic

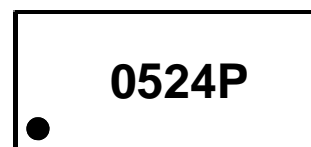
## Features

- ◆ Ultra low capacitance: 0.2pF typical (I/O to I/O)
- ◆ Ultra low leakage: nA level
- ◆ Low operating voltage: 5V
- ◆ Low clamping voltage
- ◆ Up to 4 lines protects
- ◆ Leadless flow-through package
- ◆ Complies with following standards:
  - IEC 61000-4-2 (ESD) immunity test
    - Air discharge:  $\pm 15\text{kV}$
    - Contact discharge:  $\pm 8\text{kV}$
  - IEC61000-4-4 (EFT) 40A (5/50ns)
  - IEC61000-4-5 (Lightning) : 4A(8/20 $\mu\text{s}$ )
- ◆ ROHS Compliant

## Applications

- ◆ HDMI 1.3 & 1.4, USB 2.0 & 3.0 and MDDI ports
- ◆ Monitors and flat panel displays
- ◆ Set-top box and digital TV
- ◆ Video graphics cards
- ◆ Digital video interface(DVI)
- ◆ Notebook Computers
- ◆ PCI express and Serial SATA ports

## Marking Information



0524P = Device Marking Code  
Dot denotes Pin1

## Ordering Information

Part Number	Marking	Packaging	Reel Size
DL0524P5-L	0524P	3000/Tape & Reel	7 inch

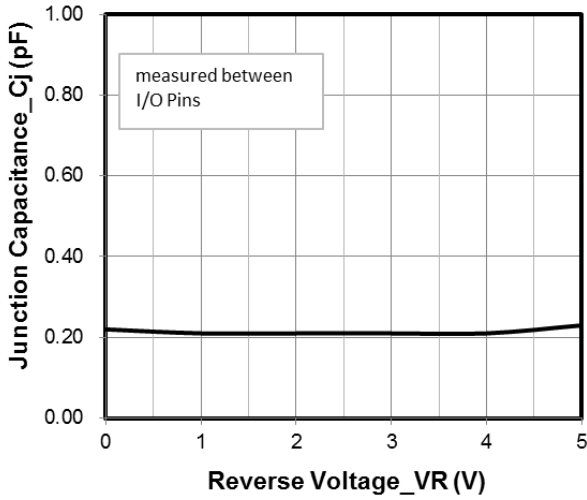
### **Absolute Maximum Ratings ( $T_A=25^{\circ}\text{C}$ unless otherwise specified)**

Parameter	Symbol	Value	Unit
Peak Pulse Power (tp=8/20μs)	PPP	60	W
Peak Pulse Current (tp=8/20μs)	I <sub>PP</sub>	4	A
ESD per IEC 61000-4-2 (Air)	V <sub>ESD</sub>	±15	kV
ESD per IEC 61000-4-2 (Contact)		±8	
Operating Temperature Range	T <sub>J</sub>	-55 to +125	°C
Storage Temperature Range	T <sub>stg</sub>	-55 to +150	°C

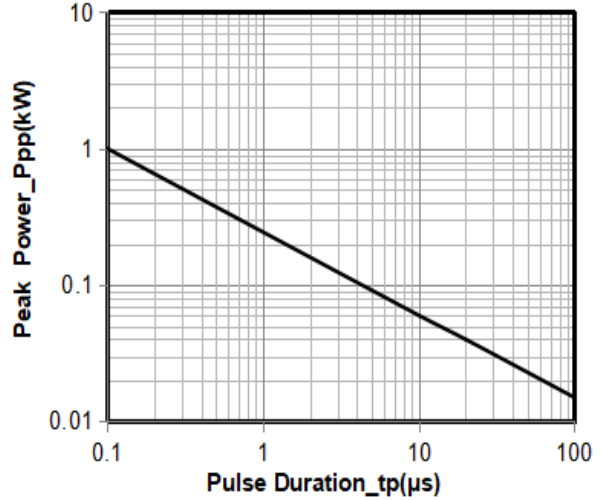
### **Electrical Characteristics ( $T_A=25^{\circ}\text{C}$ unless otherwise specified)**

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse Working Voltage	V <sub>RWM</sub>			5	V	Any I/O pin to ground
Breakdown Voltage	V <sub>BR</sub>	6			V	I <sub>T</sub> = 1mA, any I/O pin to ground
Reverse Leakage Current	I <sub>R</sub>			0.5	μA	V <sub>RWM</sub> = 5V, any I/O pin to ground
Clamping Voltage	V <sub>C</sub>			10	V	I <sub>PP</sub> = 1A (8 x 20μs pulse) any I/O pin to ground
Clamping Voltage	V <sub>C</sub>			15	V	I <sub>PP</sub> = 4A (8 x 20μs pulse) any I/O pin to ground
Junction Capacitance	C <sub>J</sub>		0.2	0.3	pF	V <sub>R</sub> = 0V, f = 1MHz, between I/O pins
Junction Capacitance	C <sub>J</sub>			0.5	pF	V <sub>R</sub> = 0V, f = 1MHz, any I/O pin to ground

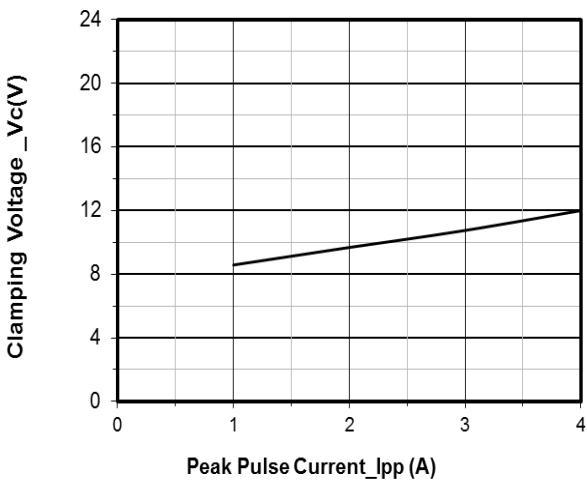
**Typical Performance Characteristics (TA=25°C unless otherwise Specified)**



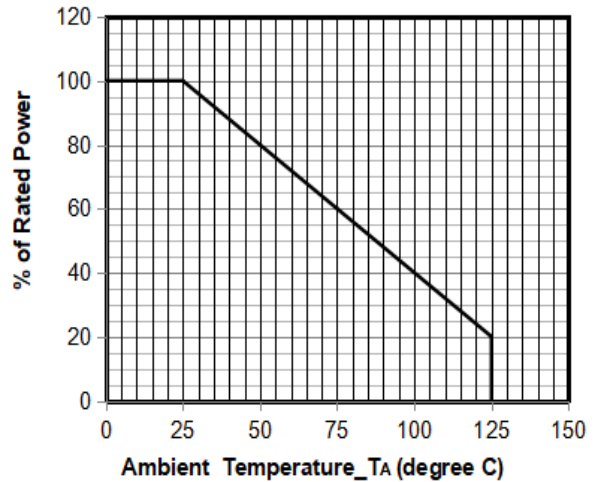
Junction Capacitance vs. Reverse Voltage



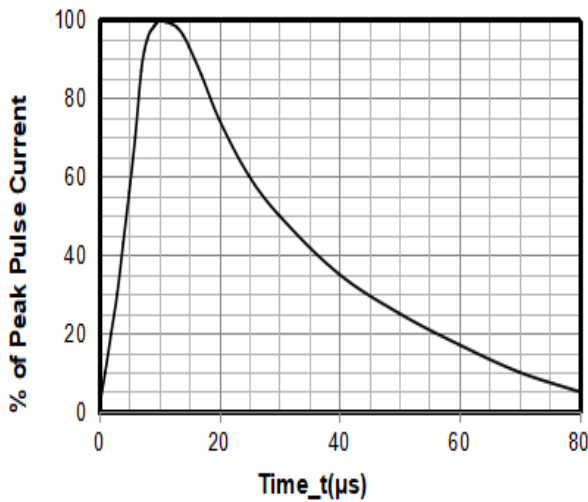
Peak Pulse Power vs. Pulse Time



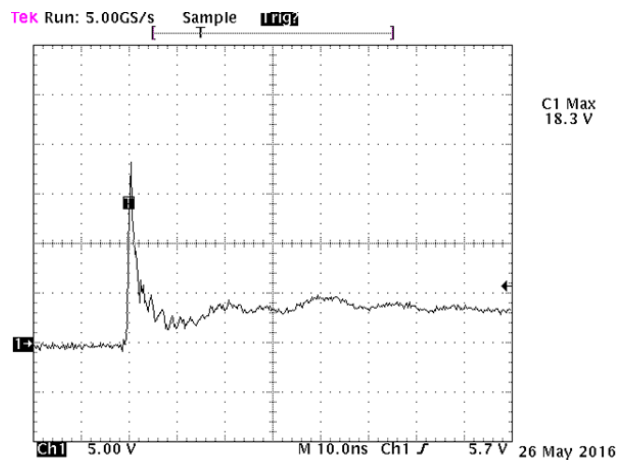
Clamping Voltage vs. Peak Pulse Current



Power Derating Curve



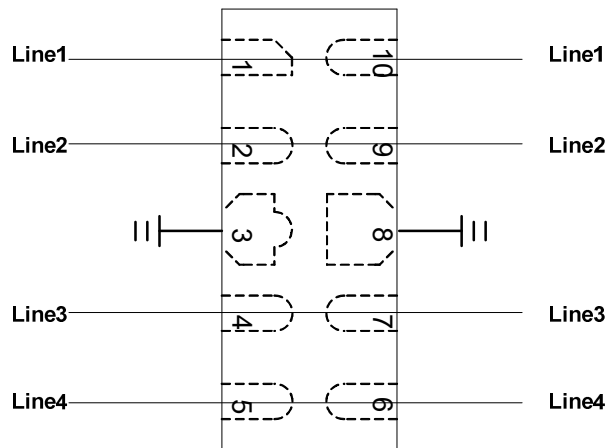
8 X 20μs Pulse Waveform



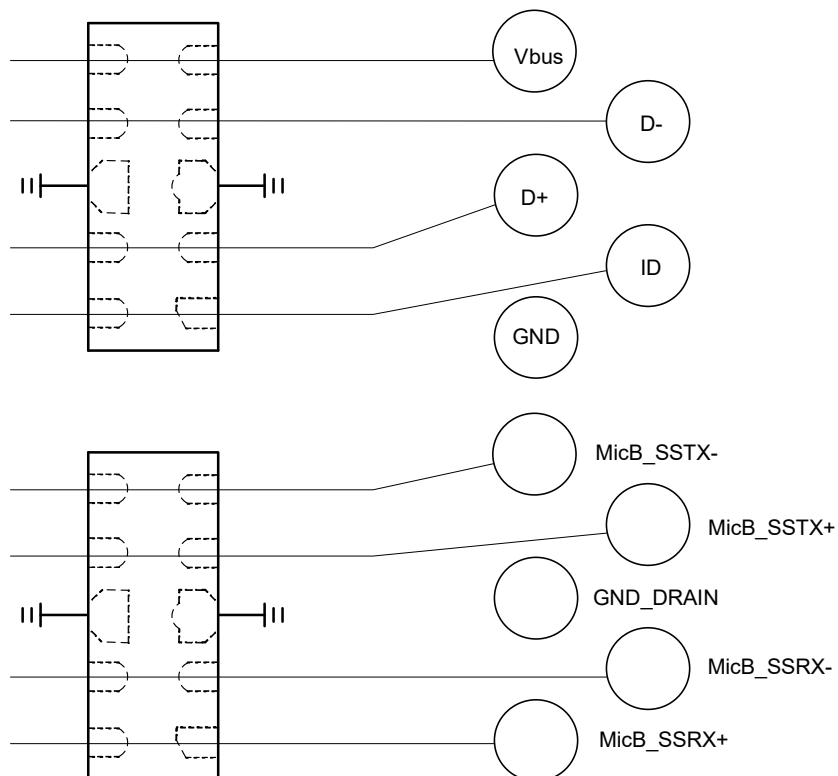
Note: Data is taken with a 10x attenuator Contact discharge current waveform per IEC61000-4-2

## Typical Application

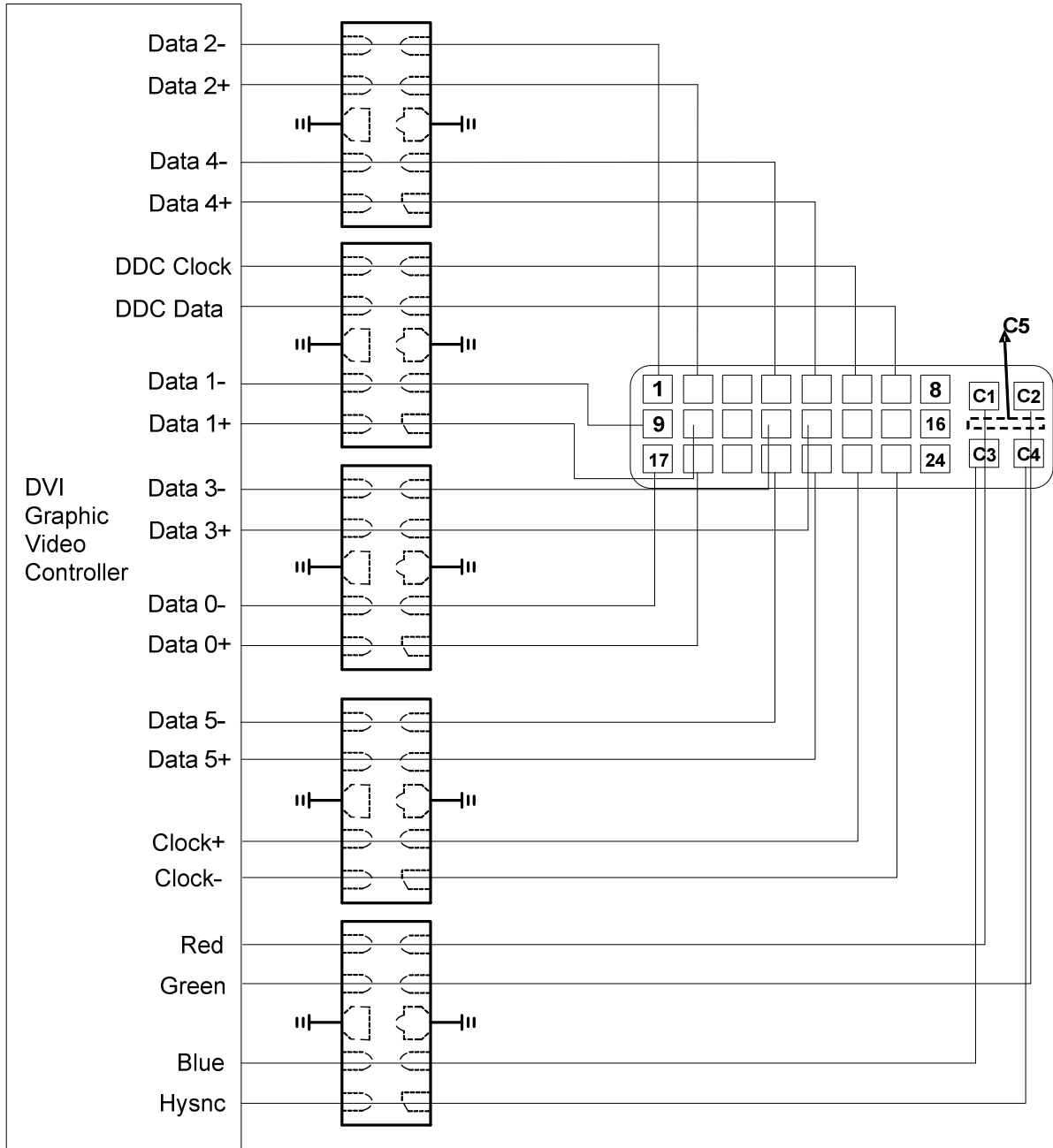
The DL0524P5-L is designed for easy PCB layout by allowing the traces to run straight through the device. The PCB traces could be used to connect the pin pairs for each line. For example, line 1 enters at pin 1 and exits at pin 10 and the PCB trace connects pin 1 and pin 10 together. Ground is connected at pin 3 and pin 8.



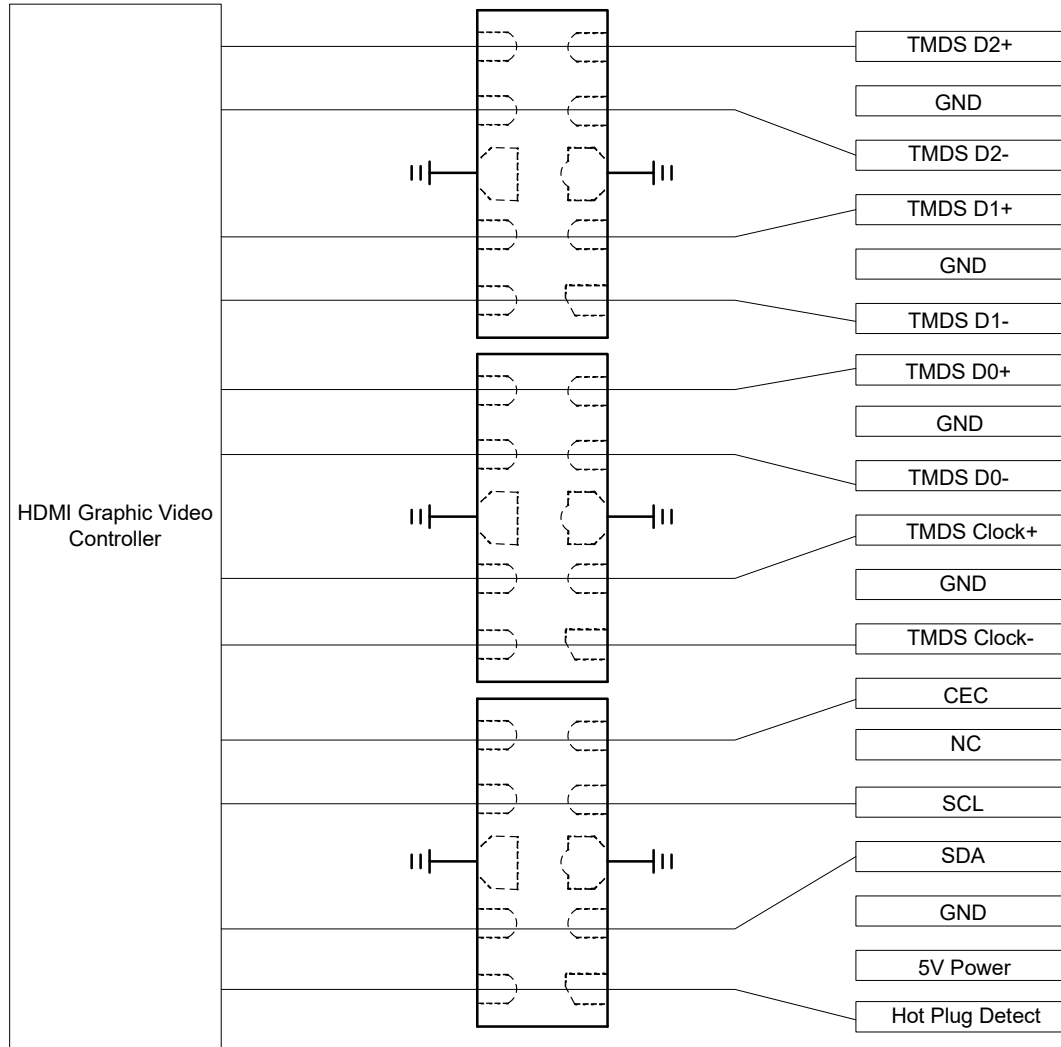
## DL0524P5-L on USB 3.0 Port Application



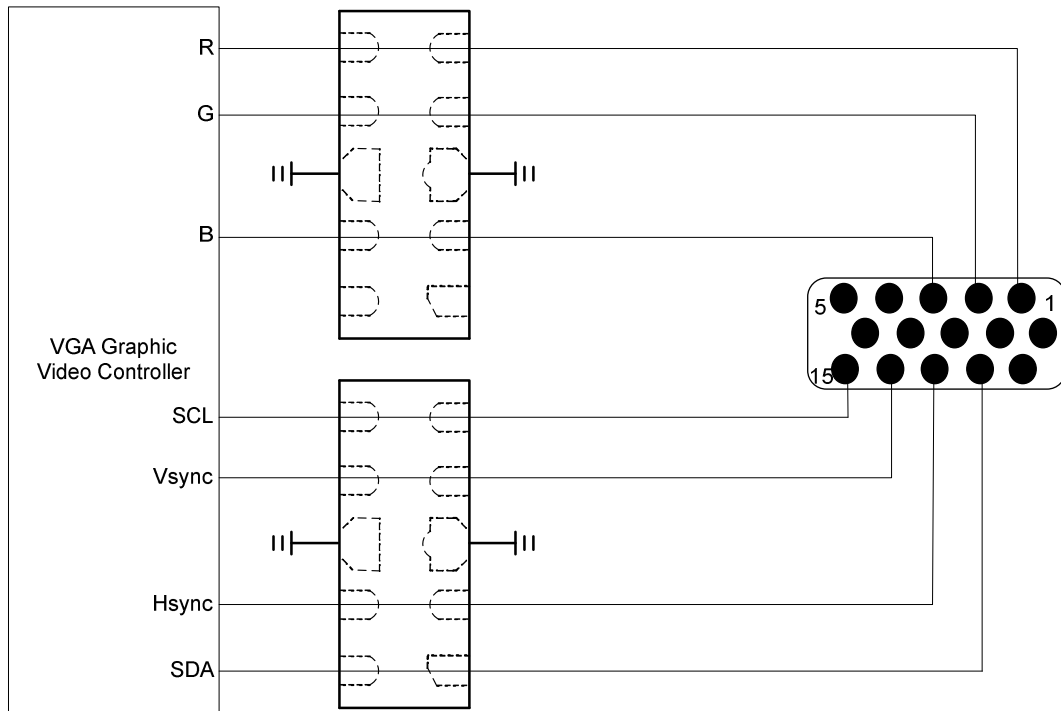
**DL0524P5-L on DVI Port Application**



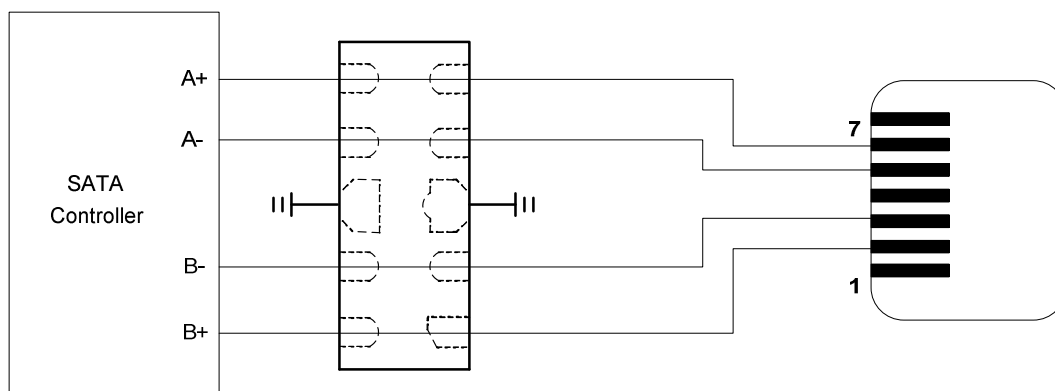
**DL0524P5-L on HDMI Port Application**



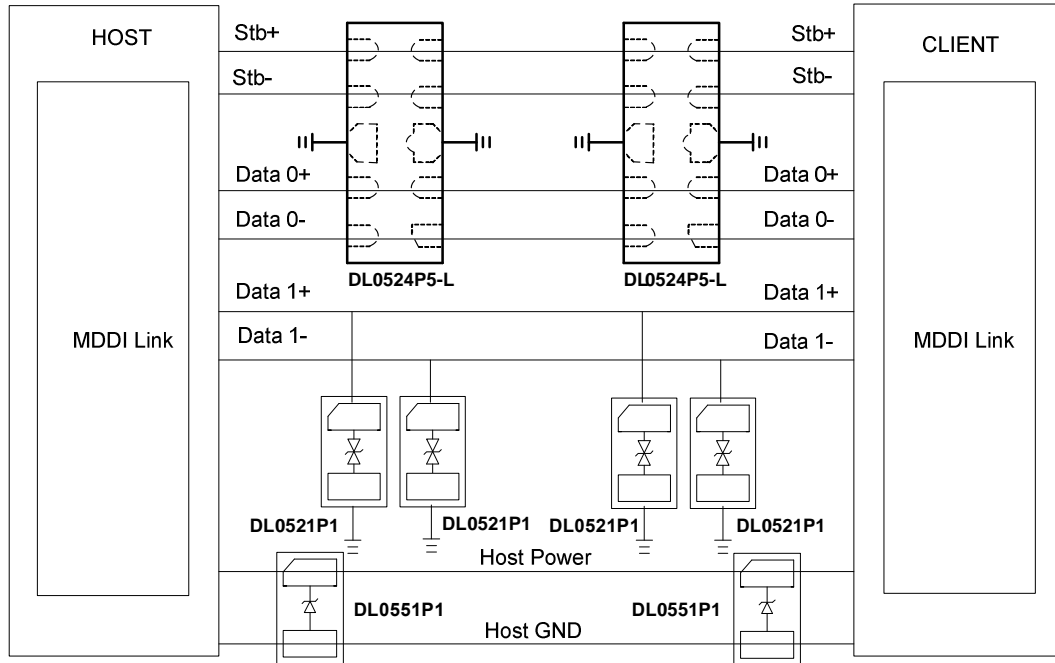
**DL0524P5-L on VGA Port Application**



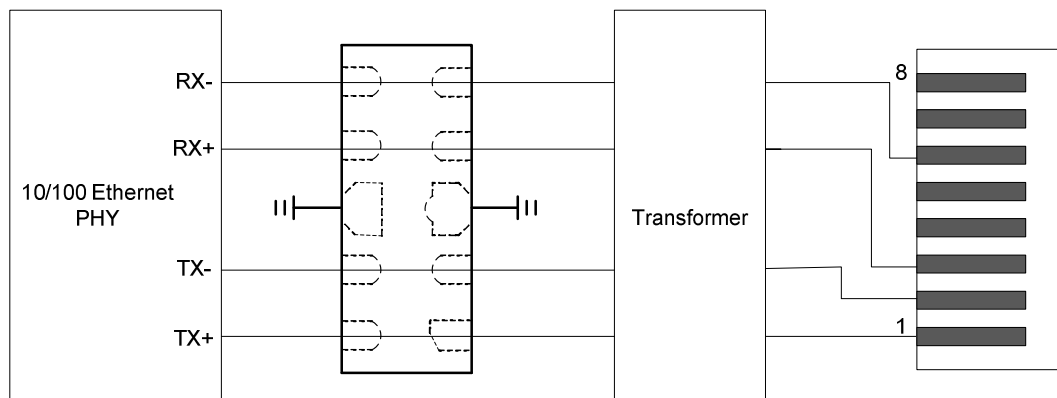
**DL0524P5-L on SATA Port Application**



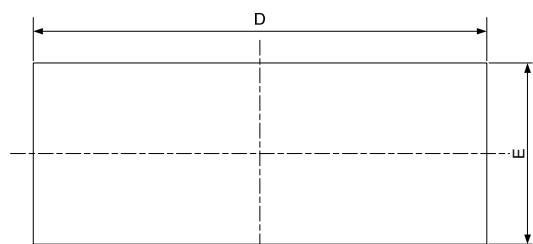
**DL0524P5-L on MDDI Port Application**



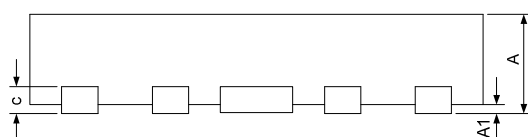
**DL0524P5-L on 10/100 Base Ethernet Port Application**



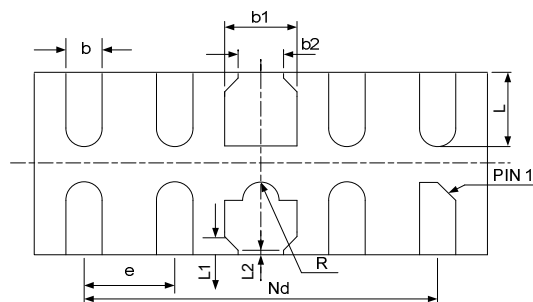
## DFN2510-10 Package Outline Drawing



TOP VIEW



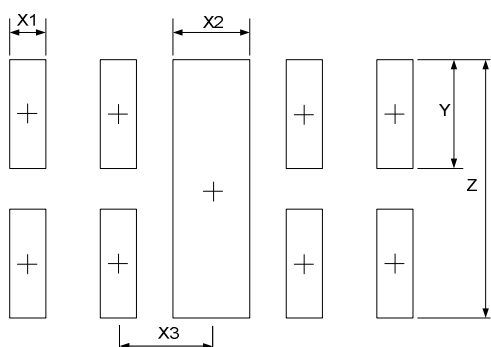
SIDE VIEW



BOTTOM VIEW

SYM	DIMENSIONS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.45	0.50	0.55	0.018	0.020	0.022
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
b1	0.35	0.40	0.45	0.014	0.016	0.018
b2	0.20	0.25	0.30	0.008	0.010	0.012
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.45	2.50	2.55	0.098	0.100	0.102
e	0.50BSC			0.020BSC		
Nd	2.00BSC			0.080BSC		
E	0.95	1.00	1.05	0.038	0.040	0.042
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.075REF			0.003REF		
L2	0.050REF			0.002REF		
h	0.08	0.12	0.15	0.003	0.005	0.006
R	0.05	0.10	0.15	0.002	0.004	0.006

## Suggested Land Pattern



SYM	DIMENSIONS	
	MILLIMETERS	INCHES
X1	0.200	0.008
X2	0.400	0.016
X3	0.500	0.020
Y	0.600	0.024
Z	1.400	0.056

## Contact Information

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